Extensible Beamformer with Dynamic Focusing for 1.5D Sonar Arrays

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LONG-TERM GOALS

Imaging sonars for divers, Unmanned Underwater Vehicles (UUVs), Autonomous Underwater Vehicles (AUVs) and torpedoes are presently limited in their resolution by the size and power consumption of their receiver/beamformer electronics. New beamforming approaches are being investigated that substantially reduce size and power and can be configured for a wide range of array geometries and operating frequencies.

OBJECTIVES

The goal for this program is to build an integrated circuit (IC) chip set for portable, high resolution, 1.5-dimensional imaging sonars. The circuitry includes dynamic focusing and is extensible from a basic tile of 32 channels forming 32 beams up to 512 azimuthal channels and beams, using coherent interpolation of both amplitude and phase information to form very high-resolution images.

APPROACH

The chip set includes an analog Front End IC, a digital Beamformer IC, and a digital Interpolation IC. Each front end channel consists of a Low Noise Amplifier (LNA), Time-Variable Gain Amplifier (TVG), and switched-capacitor Delta-Sigma Analog-to-Digital Converter (ADC). The Front End chip will be fabricated on a low-cost BiCMOS process at a commercial foundry. The Beamforming and Interpolation chips will be high-speed, high-density Field Programmable Gate Arrays (FPGAs) for low cost and flexibility in evaluation and redesign.

Key overall specifications include dynamic focusing down to three meters, 90 dB system dynamic range, and usability over a range of carrier frequencies from 100 kHz to 1 MHz.

WORK COMPLETED

Beamformer Architecture and Simulation. Two alternate digital beamforming architectures incorporating dynamic focusing were constructed and evaluated through behavorial and gate-level simulations. A structure based on delay lines was chosen for the evenly spaced linear arrays targeted by the program. A more complex but also more flexible RAM-based architecture was also demonstrated in simulations, but proved to require significantly more power. This second approach should be very attractive for curved or sparse transducer arrays, however. The delay line Beamformer

IC, which includes dynamically-focused beamsumming, demodulation, and filtering, has been successfully simulated and routed at the gate level on a Xilinx Virtex1000 FPGA up to 1 MHz carrier frequency.

We have completed gate level simulations and routing of the Interpolation FPGA. It is implemented on the Xilinx Virtex600 FPGA, which is packaged in a 240-lead quad flatpack.

We created a testbed for the Beamformer and Interpolation FPGAs by modifying a Xilinx FPGA demo board. Control, data storage, and analysis code were added to the actual FPGA program, so that the chips could test themselves in this setup. The Interpolation chip and about 30% of the beamformer chip were fully verified in the setup. This effort will be completed in the Option phase of the program.

Front End Design and Simulation. During FY00 we become aware of the impending availablility, through the DARPA-funded MOSIS foundry service, of a more suitable process, the IBM 5HP hetero-junction bipolar (HBT)/CMOS process, for the Front End Chip. Simulations of the delta-sigma ADC in the previous process gave marginal performance at a 16 MHz sampling rate, while 32 MHz was desired. Also, this previous process is only available in whole lots; the IBM 5HP process is more affordable on a project-wafer basis through MOSIS.

Hence we decided to modify and resimulate the delta-sigma modulator, which worked very well in the IBM process. The LNA and the TVG have also been simulated on the IBM process. Physical layout of the LNA and TVG blocks is nearly completed. The overall chip layout is currently being adapted from a chip designed from another ONR program, N0014-96-C-0191, which used the 5HP process. (The cost of the design of the LNA and TVG blocks was shared between these two programs, as they had similar requirements in each.)

RESULTS

The LNA has a simulated input noise of 3 nV/$\sqrt{Hz}$, a gain-bandwidth product of 500 MHz, and a dynamic range of 84 dB for a bandwidth of 50 kHz. The TVG achieves an 86 dB product of gain range times signal-to-noise ratio (SNR).

The delta-sigma ADC has a simulated SNR of greater than 66 dB (11 effective bits) for a carrier frequency of 2 MHz and a bandwidth of 100 kHz.

Simulations of the interpolation algorithm showed that sidelobes remained at -30 dB or less for up to four levels of interpolation. The combined operation of the Beamformer and Interpolation Chips has been successfully simulated at the gate level for two 32-channel sub-aperatures imaging an array of 32 staggered point sources (Figure 1).

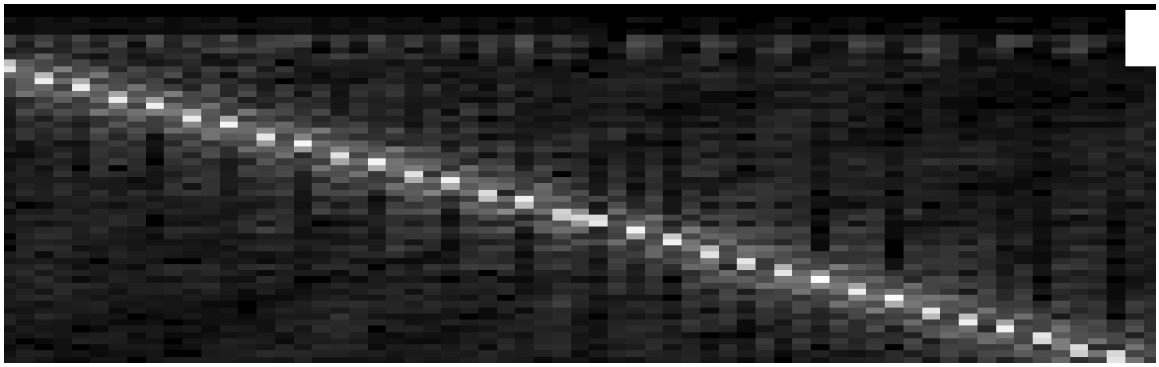

Figure 1

IMPACT/APPLICATION

This chip set is particularily suited for short range, high resolution mine detection and identification and similar diver-held sonars. It is also applicable for longer-range UUV applications utilizing linear sonar arrays. The alternative, RAM-based beamforming approach can be used for conformal transducer arrays, as for torpedoes. A particular advantage is the adaptability of the chip set to many sonar systems, reducing development and production costs.

TRANSITIONS

Sonatech Corp., a leading manufacturer of small military sonars, is a consultant on sonar requirements and architectures for this program. Sonatech plans to perform a sonar demonstration of the resulting beamformer as part of the Phase 2 option of this program.

We have opened discussions with a commercial sonar company which is interested in employing the delta-sigma ADC approach to reduce the cost of its towed imaging sonars, through increased level of integration and minimizing the number of precision components. These sonars are used primarily for hydrographic applications. Furthermore, the alternate, RAM-based beamforming approach may prove to be very suitable for their work in the areas of hull-conformal and sparse sonar arrays.

RELATED PROJECTS

Technology for Hand-Held Ultra Sound Scanners; N0014-96-C-0191.

Acoustic Video Converter; N00174-96-C-0051.

REFERENCES

T.E. Linnenbrink and S.R. Freeman, 2000. Delta-Sigma Beamforming for Sonar Imaging, Oceanic Imaging Conference 2000, Newport RI, May 4.